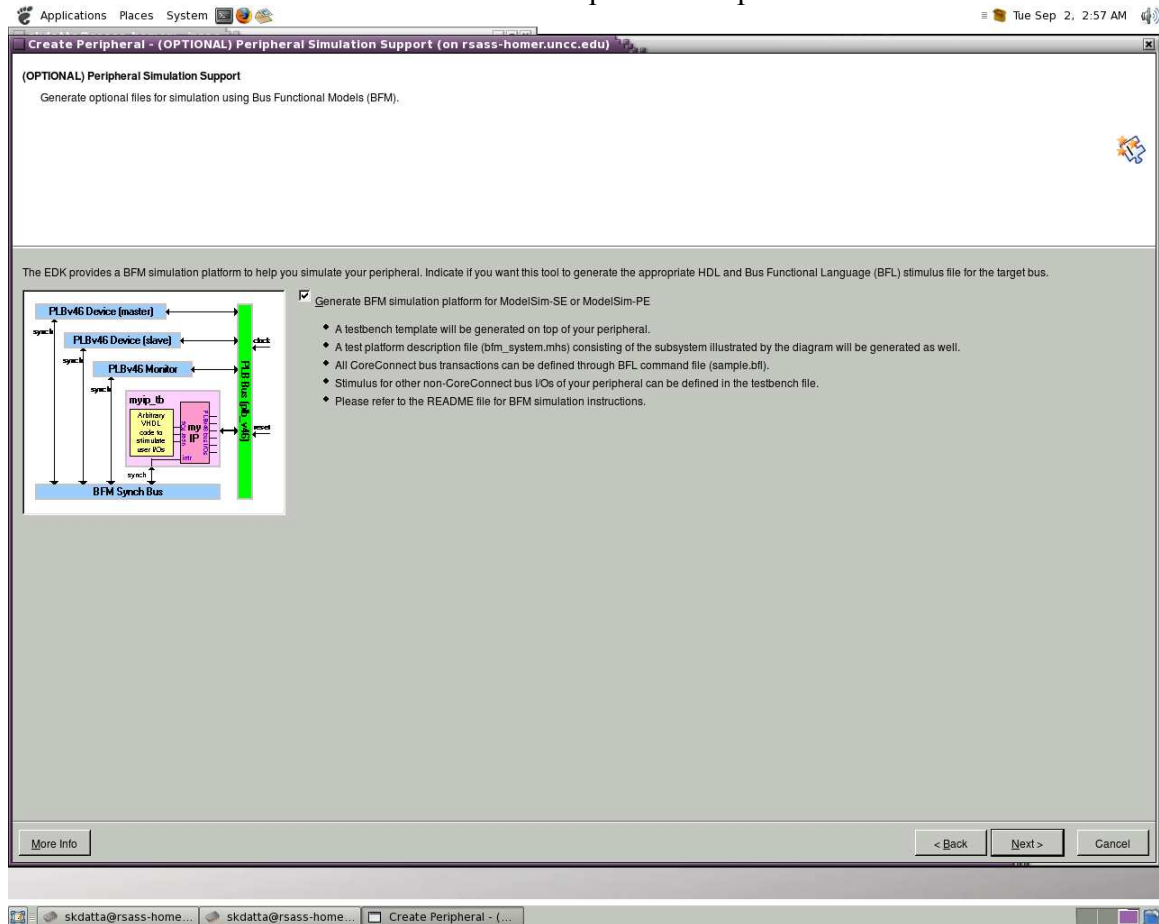


## NOTES ON USING COREGEN AND MODEL-SIM:

Steps to synchronize the component with the Bus Functional Module of Model-Sim:

1. While creating a core using Create and Import Peripheral Wizard, make sure to select the “Generate BFM simulation platform” option.



2. Once done that, you will find bfmsim in pcores/<core\_name>/devl/bfmsim.
3. In bfmsim/pcores/<core\_name\_tb\_version>/data/<core\_name\_version>.pao file, add your <component\_name>.vhd as “lib” not as “simlib”.
4. In pcores/<core\_name>/devl/bfmsim/scripts, you will find run.do, wave.do and sample.bfl
5. Change Run test time in the run.do to 10 us or 12 us. This is the file called by the Makefile.
6. In the wave.do, all the signal names are given which will show up once Modelsim is running.
7. The sample.bfl is the file where you make changes to values inserted into the slave registers of the user core. It can be modified to your core’s needs.
8. Once that’s done, run:  

```
make -f bfm_sim_cmd.make sim
```

9. This will pop up the Modelsim GUI.
10. If you make any changes to the user\_logic.vhd or the wave.do file, all you can do to recompile is to goto the command line in the GUI, press the “up arrow key” and hit enter.
11. If you make changes to the sample.bfl file, you will have to run the makefile again, but there is no necessity of closing the GUI.  
Just type `make -f bfm_sim_cmd.make` and then goto the GUI and repeat step 10.